KAMARAJ
COLLEGE OF ENGINEERING & TECHNOLOGY
(An Autonomous Institution - AFFILIATED TO ANNA UNIVERSITY, CHENNAI)
S.P.G.Chidambara Nadar - C.Nagammal Campus
S.P.G.C. Nagar, K.Vellakulam – 625 701 (Near VIRUDHUNAGAR).

Department of Electronics and Communication Engineering

Course Code	Course Name	L	T	P	C
Value Added Course	System Verilog	20	0	25	2

a. Preamble

This course delves into the solid foundation in Register Transfer Level (RTL) design and modern verification methodologies in VLSI (Very Large Scale Integration). Through hands-on labs and real-world examples, learners will explore the construction of testbenches, assertion-based verification, and functional coverage. Emphasis is placed on building skills that align with current industry standards and expectations. The course is ideal for students aiming for careers in semiconductor design and manufacturing

b. Course Outcome

Upon successful completion of the course, the students will be able to

COs	Course Outcome	Knowledge Level
CO1	Understand RTL design and verification techniques	K2
CO2	Hands-on experience with System Verilog constructs Exposure to real-world testbenches and functional coverage	K3

Introduction to System Verilog & Digital Design Concepts **5 Hours**

Overview of System Verilog and its role in verification - Difference between Verilog and System Verilog - Data Types and Operators - Modules, Interfaces, Ports

Procedural Coding and Hierarchical Modeling **5 Hours**

Procedural Blocks: initial, always, forever-Blocking vs Non-blocking assignments -Hierarchical Design & Testbench Basics

Verification Methodology & Functional Coverage **10 Hours**

Classes, Objects, Constructors Inheritance and Polymorphism Randomization Concepts: rand, randc, constraints Transaction-Level Modeling (TLM) - Functional Coverage – covergroups, coverpoints

Finite State Machines and Protocol Verification **10 Hours**

FSM Design and Verification using System Verilog - Bus Protocol Example (e.g., AXI-lite / I2C / SPI) - Implement and verify a protocol using assertions and coverage

Projects & Assignments **15 Hours**

Mini Project: Design & Verification

- UART
- FIFO
- Traffic Light Controller

CO – PO mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1: Understand RTL design and verification techniques (K2)	3	2	2	2	3	-	-	-	-	2	-	2	3	2
CO2: Hands-on experience with System Verilog constructs, testbenches & coverage (K3)	3	3	3	3	3	-	-	-	2	3	2	3	3	3

SDG Mapping

COs	Relevant SDGs
CO1: Understand RTL design and verification techniques (K2)	**SDG 4** (Quality Education), **SDG 9** (Industry, Innovation & Infrastructure)
CO2: Hands-on experience with System Verilog constructs, real-world testbenches & coverage (K3)	**SDG 4** (Quality Education), **SDG 8** (Decent Work & Economic Growth), **SDG 9** (Industry, Innovation & Infrastructure)